complex. Moreover, when the electrode layer is made of a material, such as tantalum, a tantalum alloy, a tantalum nitride, or any other kind of tantalum compound, it is difficult to perform etching because such material is chemically stable. Also, the hardness level of such material is high and, therefore, mechanical polishing performed on this material is not as easy as on copper or a copper alloy that is a wiring material. When, for instance, the hardness level of abrasive grain is raised too high in order to increase a polishing rate during the CMP process, a polishing flaw may be caused and this may result in faulty electrical characteristics. Furthermore, when the grain concentration of an abrasive used in the CMP process is increased, this increases a polishing rate for a silicon dioxide film or the like that is an insulating film, thereby resulting in erosion (i.e., surface damage).

**[0010]** The present invention is conceived to solve the stated conventional problem, and has an object to provide: a method of manufacturing a non-volatile semiconductor memory element suited to miniaturization, able to be manufactured by an easy process, small in element-to-element variations, capable of a stable operation, and suited to capacity enlargement and a high degree of integration; and a method of manufacturing a non-volatile semiconductor memory device.

## Solution to Problem

**[0011]** In order to achieve the aforementioned object, the method of manufacturing the non-volatile semiconductor memory element in an aspect according to the present invention is a method of manufacturing a non-volatile semiconductor memory element including a variable resistance element and a non-ohmic element connected in series with the variable resistance element, the variable resistance element including (i) a first electrode, (ii) a variable resistance layer formed on the first electrode, and (iii) a shared electrode formed in an upper part of the variable resistance layer, the non-ohmic element including (i) the shared electrode, (ii) one of a semiconductor layer and an insulator layer formed on the shared electrode, and (iii) a second electrode formed on the one of the semiconductor layer and the insulator layer, and the method including: forming the first electrode on a substrate; forming the variable resistance layer on the first electrode, the variable resistance layer comprising a transition metal oxide; forming the shared electrode by nitriding a front surface of the variable resistance layer; forming the one of the semiconductor layer and the insulator layer on the shared electrode; and forming the second electrode on the one of the semiconductor layer and the insulator layer, wherein, in the forming of the shared electrode, a front surface of the transition metal oxide is nitrided according to a plasma nitriding process so as to form the shared electrode comprising a transition metal nitride.

**[0012]** In the case of the method of manufacturing a shared electrode according to a conventional filling process, a series of processes are performed to: form a concave part by eliminating a part of the variable resistance layer formed inside the memory cell hole, by, for example, overpolishing or dry etching; and form an electrode film and then eliminate an unnecessary part of the electrode film by the CMP process. On the other hand, according to the manufacturing method according to the present invention, the oxygen atoms in the variable resistance layer are replaced by the nitrogen atoms only via the plasma nitriding process. Therefore, a method of manufacturing a non-volatile semiconductor memory device can be simplified. Moreover, since the CMP process does not need to be repeated, the front surface of the electrode layer is flat and thus variations in device characteristics can be reduced.

**[0013]** Furthermore, the shared electrode formed by the nitriding process according to this manufacturing method has a high barrier property against oxygen diffused from the variable resistance layer comprising the transition metal oxide to the semiconductor or insulator layer. Thus, the film thickness can be reduced as compared with the conventional shared electrode, meaning that the present shared electrode is useful in miniaturization. In particular, a shared electrode layer having a high nitrogen density can be formed at a low temperature by using the plasma nitriding process as a nitriding process. This improves the barrier characteristics, and the shared electrode can be thus thinned. Moreover, the plasma nitriding method can uniformly control a plasma distribution state by an external magnetic field effect. Thus, variations in film thickness of the shared electrode can be reduced by high in-plane uniformity, thereby significantly reducing in-plane variations in characteristics of the non-volatile memory element.

**[0014]** Moreover, it is preferable for the transition metal oxide to be one of a tantalum oxide and a hafnium oxide, and it is preferable for a front surface of the one of the tantalum oxide and the hafnium oxide to be nitrided so as to form the shared electrode comprising a corresponding one of a tantalum nitride and a hafnium nitride.

**[0015]** Furthermore, the variable resistance layer may include: a first transition metal oxide layer formed on the first electrode; and a second transition metal oxide layer that is formed on the first transition metal oxide layer and has a lower oxygen content atomic percentage than the first transition metal oxide.

**[0016]** This configuration can implement a non-volatile memory element that uses a resistance change phenomenon and has a property of performing reversibly stable rewriting.

**[0017]** The method of manufacturing the non-volatile semiconductor memory device in an aspect according to the present invention is a method of manufacturing a cross point non-volatile semiconductor memory device including a plurality of non-volatile semiconductor memory elements arranged in an array, each of the non-volatile semiconductor memory elements having a variable resistance element and a non-ohmic element connected in series with the variable resistance element, the variable resistance element including (i) a lower electrode line formed to be shared by, among the non-volatile semiconductor memory elements arranged in the array, non-volatile semiconductor memory elements arranged in a first direction, (ii) a variable resistance layer formed on the lower electrode line, and (iii) a shared electrode formed in an upper part of the variable resistance layer, the non-ohmic element including (i) the shared electrode, (ii) one of a semiconductor layer and an insulator layer formed on the shared electrode, and (iii) an upper electrode formed on the one of the semiconductor layer and the insulator layer, and the method including: forming, on a substrate, a plurality of lower electrode lines in parallel in the first direction; forming an interlayer insulating layer on the substrate including the lower electrode lines; forming a plurality of memory cell holes in the interlayer insulating layer formed on the lower electrode lines; filling a transition metal oxide included in the variable resistance layer into the memory cell holes; forming the shared electrode by nitriding a front surface of the variable